2008 Analog Decoding Workshop

July 12, 2008 – Logan, Utah, USA

Hosted by
Electrical and Computer Engineering Department
Utah State University
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<th>Author(s)</th>
<th>Affiliation</th>
<th>Title</th>
</tr>
</thead>
<tbody>
<tr>
<td>8:30 AM</td>
<td>Continental Breakfast</td>
<td></td>
<td></td>
</tr>
<tr>
<td>9:30 AM</td>
<td>C. Winstead and K. Payak</td>
<td>Utah State</td>
<td>Gate Complexity and Power Consumption of Stochastic Iterative Decoders</td>
</tr>
<tr>
<td>10:00 AM</td>
<td>S. Sharifi Tehrani, S. Mannor and W. Gross</td>
<td>McGill</td>
<td>A Novel Architecture for Fully-parallel Stochastic LDPC Decoders</td>
</tr>
<tr>
<td>10:30 AM</td>
<td>N. Nguyen, C. Myers, H. Kuwahara, and C. Madsen</td>
<td>U. of Utah</td>
<td>Dynamics of Analog Decoders for Different Message Representation Domains</td>
</tr>
<tr>
<td>11:00 AM</td>
<td>S. Hemati and A. Yongacoglu</td>
<td>U. of Ottawa</td>
<td></td>
</tr>
<tr>
<td>11:30 AM</td>
<td>LUNCH BREAK</td>
<td></td>
<td></td>
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<tr>
<td>1:00 PM</td>
<td>M. Zargham, V. Gaudet and C. Schlegel</td>
<td>U. of Alberta</td>
<td>Limitations on Analog Decoder Performance due to CMOS Scaling</td>
</tr>
<tr>
<td>1:30 PM</td>
<td>S. M. Reza Dibaj and F. Lahouti</td>
<td>U. of Tehran</td>
<td>An Analog Circuit for Implementation of Arithmetic Coding</td>
</tr>
<tr>
<td>2:00 PM</td>
<td>S. Howard and P. Flikkema</td>
<td>Northern Arizona</td>
<td>Combined Source-Channel Decoding and Transmission Censoring for Power Reduction in a Wireless Sensor Network</td>
</tr>
<tr>
<td>2:30 PM</td>
<td>15 MIN. BREAK</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2:45 PM</td>
<td>M. Gu and S. Chakrabartty</td>
<td>Michigan State</td>
<td>Stochastic Resonance in Margin Propagation Based Analog Decoders</td>
</tr>
<tr>
<td>3:15 PM</td>
<td>C. Winstead, B. Eames and M. Phadnis</td>
<td>Utah State</td>
<td>Density Propagation Techniques for Optimizing Mixed-Signal Systems</td>
</tr>
<tr>
<td>3:45 PM</td>
<td>C. Schlegel, V. Gaudet and R. Dodd</td>
<td>U. of Alberta</td>
<td>Iterative Cancellation</td>
</tr>
<tr>
<td>4:00 PM</td>
<td>ADW09 Planning Session</td>
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<tr>
<td>4:30 PM</td>
<td>Recess until dinner</td>
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<td></td>
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<tr>
<td>6:00 PM</td>
<td>Dinner at Blackstone (meet at University Inn)</td>
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We present results on transistor-level implementations for components used in typical stochastic decoding architectures. Example designs are presented for counter and shift-register edge memory schemes. Using Spectre simulations, the transistor count and power consumption are measured for each type of component. These results are then used to project power consumption and transistor count for various LDPC stochastic decoders. The results show that the dual counter architecture requires almost 1000 more transistors per edge memory than the shift-register scheme, but the dual counter version uses roughly 1/4th the power required by the shift register method. Therefore the two methods offer a significant trade-off between transistor count and power consumption.

The dual counter edge memory has an 8-bit resolution with a pipelined bit-stream generator. The shift-register edge memory has a length of 32 bits, and uses a 5-bit random number generator and a 32:1 multiplexer to implement random addressing. These parameters correspond to typical values presented at previous meetings of the Analog Decoding Workshop. For benchmarking, a 0.6um process was used. The transistor counts and relative power consumption trends should remain the same in other technologies.
Saeed Sharifi Tehrani, Shie Mannor and W. Gross,
“A Novel Architecture for Fully-parallel Stochastic LDPC Decoders”
Department of Electrical and Computer Engineering
McGill University, 3480 University Street, Montreal, Quebec, Canada H3A 2A7
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Stochastic decoding is an alternative method for low complexity decoding of error-correcting codes. This paper discusses the first hardware architecture for stochastic decoding of practical state-of-the-art Low-Density Parity-Check (LDPC) codes on factor graphs. This architecture is used to implement a (1024,512) fully-parallel LDPC decoder on a Xilinx Virtex-4 XC4VLX200 FPGA device. The implemented decoder occupies about 36% of the FPGA device which shows about 53% more area efficiency (measured as FPGA Slices per coded bit) compared to the recent FPGA-based bit-serial Min-Sum decoder in [1]. The decoder achieves a clock frequency of 212 MHz and provides a throughput of 706 Mbps at $E_b/N_0 = 3$ dB (bit-error-rate of about $10^{-6}$). The decoding performance of the decoder is within 0.2 dB of floating-point sum-product algorithm with 32 iterations and significantly outperforms MinSum decoding.

Table I: Components Used in the Decoder and the Implementation Results on a Xilinx Virtex-4 XC4VLX200 Device

<table>
<thead>
<tr>
<th>Module</th>
<th>Number used in the decoder</th>
<th>Area Occupation (Virtex-4 Slices)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Comparator</td>
<td>1024</td>
<td>6</td>
</tr>
<tr>
<td>Up/Down Counters</td>
<td>1024</td>
<td>6</td>
</tr>
<tr>
<td>Degree-3 variable nodes</td>
<td>1024</td>
<td>10</td>
</tr>
<tr>
<td>Degree-6 check nodes</td>
<td>512</td>
<td>5</td>
</tr>
<tr>
<td>Randomization Engine</td>
<td>1</td>
<td>394</td>
</tr>
<tr>
<td><strong>Stochastic Decoder</strong></td>
<td>−</td>
<td><strong>32875 (36%)</strong></td>
</tr>
</tbody>
</table>

Reference

Synthetic biology is the study of genetically engineering new biological pathways that can potentially change the behavior of organisms in useful ways. Crucial to the research efforts in synthetic biology are the construction of new, complex genetic circuits. Genetic circuits have stochastic behavior, and therefore must be robust to noise.

This talk presents an example of a genetic circuit, the genetic Muller C-element. The Muller C-element is a standard component used in asynchronous circuit design to synchronize signals. The function of the Muller C-element is identical to that of the equality gate used in stochastic iterative decoders. The Muller C-element has two inputs and one latched output. The output is driven high when both the inputs are high, and is driven low when both the inputs are low. If the two inputs are not equal, the latched output does not change.

This talk discusses the parallels between design in a genetic environment and in an analog environment and further explores the relationship between the genetic Muller C-element and the stochastic equality gate.
Saied Hemati and Abbas Yongacoglu,
“Dynamics of Analog Decoders for Different Message Representation Domains”
School of Information Technology and Engineering
University of Ottawa
Ottawa, Canada
Email: {Hemati, yongacog}@site.uottawa.ca

We study analog decoders in an abstract level and show that their dynamic equations change with message representation domain. This result, which is in contrast with behavior of conventional discrete-time iterative decoders, is derived based on the continuity requirement for messages that are passed between processing nodes in analog decoders.
This talk will review a number of transistor non-idealities in sub-100nm CMOS technologies (DIBL, leakage, mismatch), and their impact on the performance of analog decoders that are designed using them. Overall, mismatch will impose the most significant limitation on scaling. Guidelines for transistor sizing in these technologies will be provided.
Entropy coders are one of the important components of most compression standards. Specifically, arithmetic coding provides a high compression performance and is a key element for improved coding efficiency of recent multimedia communication standards such as H.264, and JPEG2000. However, efficient implementation of arithmetic codes in different applications is challenging.

At the arithmetic encoder, each symbol corresponds to an interval proportionate to its probability within an area updated by its preceding symbols. The bits transmitted are obtained based on a point within this interval. The important arithmetic encoding tasks include (disregarding source modeling): (a) Interval update and arithmetic operations, (b) Carry propagation and bit moves and (c) Interval renormalization.

In this work, inspired by the recent progress in channel decoding based on analog circuits, we present an analog circuit for implementation of binary arithmetic codes that facilitates a reduced circuit complexity and a higher speed when compared to the digital counterparts. The proposed solution is motivated by the iterative nature of the arithmetic coding algorithm. Specifically, the scheme performs the interval splitting by a simple resistance divider. Switches, based on the input symbols, select one of the resistance divider outputs for charging a capacitor that acts as an analog memory. This, together with the divider circuit, iteratively updates the arithmetic code intervals. Because of the limited practical precision of the circuit components, we consider a recently presented block implementation of arithmetic coding [1] to restart the en/decoding process periodically and avoid any potential errors.

The decoding is performed by reproducing the encoding process, the difference is only in the symbol search. The symbol search can be done simply by using a comparator circuit that compares the received codeword with the cumulative distribution of symbols.

Our simulations show that the time needed to encode one bit, using the proposed analog arithmetic coder, is less than 2ns. The best reported time to accomplish the same task based on a digital implementation of arithmetic coding is about 20ns [2]. Moreover, the complexity of the analog implementation is substantially smaller, as a digital implementation is challenging due the required multiplication and renormalization operations [3]. However, the limited precision of analog components requires a constrained input block length, and hence affects the possible compression gains. Specifically, considering a random error of $10^{-4}$ in the circuit elements, we assumed a short input block of 10 bits. In this case, the
reduction of compression rate of the employed block arithmetic coding with respect to entropy, is between 5% to 10%, corresponding to highly skewed and uniform binary input distributions, respectively.

References:


Sheryl Howard and Paul Flikkema,
“Combined Source-Channel Decoding and Transmission Censoring for Power Reduction in a Wireless Sensor Network”
Department of Electrical Engineering
Northern Arizona University
Flagstaff, AZ, USA
Sheryl.Howard@nau.edu

Reduction of power consumption in a wireless sensor network is crucial to the network's viability, as sensors are often battery-powered and located in remote areas. Error-correction coding (ECC) is a classic technique for reducing power consumption and retransmissions.

Environmental sensing networks typically exhibit high correlation between data samples. This source correlation can be utilized to improve performance. The authors previously examined a combined source-channel decoder (iterative and non-iterative) wherein an inference algorithm incorporating the source probabilities improves performance over ECC alone.

This work explores power reduction in a relay network, through transmission censoring. Each sensing node samples and transmits its own data, and forwards received data from its preceding node. Correlated data permits transmission censoring based on the decoder’s ability to reconstruct missing data using the source probabilities.

The current node estimates the next node's decoding decision, using the source-based inference algorithm, and code/channel knowledge. If this estimate recovers the censored data correctly, the node then censors that data, reducing transmit power. Otherwise, the data is not censored.

Results show a significant reduction in data transmitted (80% of data censored in a good channel) with minimal performance loss, for a three-node relay network with highly-correlated data (cross-correlation coefficient r=0.9).
“Noise” is typically considered a limiting factor in many engineering systems. However, it has been demonstrated that biological systems overcome some of these fundamental limitations by using “noise” as a computational resource. The core of noise-assisted computation, stochastic resonance (SR) being one such example, are non-linear response of biological computational units (neurons) which can detect sub-threshold signals buried in ambient noise. Even though sub-threshold signal detection techniques have been extensively studied in the neuroscience literature, it is still not clear how these methods translate towards constructing large scale analog decoding networks. In this work we present some preliminary results on how noise inherent in the computational elements (labeled as secondary noise) affects the performance of a low-density parity check (LDPC) analog decoder based on margin propagation. Since threshold operation is inherent in margin propagation, our results indicate an SR phenomenon whereby addition of random white noise or adaptation of the threshold parameter improves the bit error rate performance of the decoder (Both the cases are illustrated by figures below).
We present a method for using probability density propagation to forecast the reliability and yield of analog and mixed-signal circuits. Our method applies model-based signal processing [1] for use in an Electronic Design Automation (EDA) optimization tool. Beginning with an analog or mixed-signal circuit, a factor graph model is extracted. The factor graph includes error terms that arise from parametric variation in the analog components. Densities are propagated throughout the factor graph using the standard message-passing approach. By specifying statistical constraints on one or more signals in the graph, the system’s yield is predicted.

Our factor graph simulator is glued to an existing design optimization tool. In its current form, the tool optimizes a system by choosing from among several embodiments of each system component. The tool rapidly arrives at a design node which is optimized for “composable properties”, which include power consumption, area, cost and discrete failure probability. Once a candidate design node is selected, density propagation is used to verify the yield constraint for analog sub-circuits.

Previous optimization methods predicted analog yield by propagating statistical information through a circuit model. These approaches included mean and variance propagation, and sample set histograms [2]. The factor graph approach provides a unifying framework for density-propagation methods.

We consider applying density propagation to mixed-signal systems by modeling each analog signal and error source as a Gaussian mixture. Each discrete signal is modeled by a probability mass. We present some example circuits, and suggest a key problem for future research: can density propagation be used to infer component error tolerances based on system constraints? Backward inference would provide a significant benefit that is not provided by existing density propagation methods.

References:


We will discuss iterative demodulation algorithms, and present initial results of an FPGA implementation study. Since most operations involve simple summation, our long-term vision is to realize these algorithms using suitable analog circuits.
**Dining Schedule**

**Friday, July 11 – Dinner**
Workshop participants arriving on July 11 may join us for dinner at Kamin Thai restaurant. We will meet at the University Inn at 6:30PM. A University van will transport guests to the restaurant.

**Saturday, July 12 – Lunch**
Two University vans will be provided for restaurant transportation during the Saturday lunch break. Some of the local restaurant options are as follows (fast options are in bold):

- American/Sandwiches:
  - Great Harvest – Deli sandwiches
    55 W. Center St.
  - Bluebird Restaurant – Hot sandwiches, hamburgers, American entrees
    19 N. Main St.
  - Center Street Grill – Hot sandwiches and hamburgers
    18 E. Center St.
  - Chilis
    1427 N. Main St.

- Mexican:
  - El Toro Viejo
    1079 N. Main St.
  - Café Sabor – Southwest American style
    600 W. Center St.
  - Café Rio – Deli style Mexican food
    1460 N. Main St.

- Italian:
  - Olive Garden
    1220 N. Main St.

- Sushi:
  - Happy Sushi
    20 W. 400 N.

**Saturday, July 12 – Dinner**
The workshop dinner is scheduled for 6:30 PM at Blackstone restaurant, 255 S. Main St. Two University vans will be available to transport guests from the University Inn to the restaurant. We will meet at the University Inn at 6:00 PM.
Wireless Internet Access
Utah State provides wireless internet access to visitors via the “BLUEZONE-GUEST” network. To access the internet, simply connect to this network and enter the access code. Each access code is valid for one day only. Here are the codes for use during ADW08:

- Friday, July 11: cakkineth
- Saturday, July 12: shehush
- Sunday, July 13: bruchey

Navigating in Logan
Like most Utah cities, Logan uses a Cartesian addressing system. The primary axes are Center St. and Main St. Most addresses are written with reference to these axes. For example, the address “500 N. 300 E.” means “5 blocks North of Center St. and 3 blocks East of Main St.” This address is shown in the map below:

Most roads in Logan follow a grid pattern, making it very easy to find any location based on the coordinate address. Visitors should be aware that the Cartesian system is not always handled correctly by mapping services like Google maps. If you plan to drive in Utah, be sure to double-check any routes generated by Google maps to ensure that they agree with basic geometric reasoning.
Regional Attractions
Logan is situated in the heart of the American West, and many visitors are drawn to the area’s outdoor attractions. Some local day-trip activities are listed below. If several workshop participants are interested in one of these activities, a group trip can be arranged.

- **Boating / water skiing on Bear Lake:**
  contact Cisco’s Landing for boat rental information.
  - Phone: 435-946-2717

- **Canoeing / kayaking in Logan’s wetland reserve**
The “wetland maze” is home to many endangered bird species, and is a popular attraction for birdwatchers. Muddy Road Outfitters provides boat rental and a 2-hour self-guided canoe tour of Bear River.
  - Phone: (435) 213-0504
  - About the wetland maze: [http://www.bridgerlandaudubon.org/wetlandsmaze/](http://www.bridgerlandaudubon.org/wetlandsmaze/)

- **Scenic Canyon Drive**
Logan Canyon is considered to be one of the most scenic drives in the US. The canyon highway begins at the Utah State campus and runs for about 45 minutes through Utah’s alpine landscape. At the top of the canyon there is a breathtaking overlook of Bear Lake, a large turquoise-colored natural lake that straddles the Utah/Idaho border.

- **Hiking in Logan Canyon**
Logan Canyon is a popular destination for hikers and rock climbers. The canyon has many trails ranging from easy to advanced. Popular hikes include Naomi Peak, the largest point in the Bear River mountain range; and the Riverside trail, a relatively flat trail that winds around the dams and reservoirs in Logan canyon.
  - Web: [http://www.go-utah.com/Logan/Hiking/](http://www.go-utah.com/Logan/Hiking/)

Salt Lake Area Attractions:

- **World’s Largest Pit**
The Bingham Copper Mine is the world’s largest man-made object, and is visible from space. It is located at the west end of the Salt Lake valley, and is roughly a ½ hour drive from the city center. The visitor center is open daily from 8am to 8pm. Maps and other information are available of the Kennecott Mining Company’s web site.
  - Web: [http://www.kennecott.com](http://www.kennecott.com)

- **Utah’s Museums**
  - Fine Arts: [http://www.umfa.utah.edu/](http://www.umfa.utah.edu/)
  - Natural History: [http://www.umnh.utah.edu/](http://www.umnh.utah.edu/)