



# ***A Novel Architecture for Fully-Parallel Stochastic LDPC Decoders***

**Saeed Sharifi Tehrani, Shie Mannor, and Warren J. Gross**

McGill University  
Montreal, Quebec, Canada

Analog Decoding Workshop (ADW 2008)

July 12, 2008

# *LDPC Codes*

- Standards:
  - DVB-S2
  - IEEE 802.3an (10GBASE-T)
  - IEEE 802.16e (WiMAX)
  - IEEE 802.11n (WiFi)
- Turbo-like codes, but massively parallel
  - Near-capacity reaching
  - Iterative decoding with interleaver

# Goals

- **Very high-throughput LDPC decoders**
  - Fully-parallel
  - Routing congestion
  - Bit-serial message passing
- **Correct as many errors as possible**
  - Avoid the min-sum approximation
  - Use the sum-product algorithm
- **Easy (and portable) design process**
  - Digital, standard-cell

# Stochastic representation

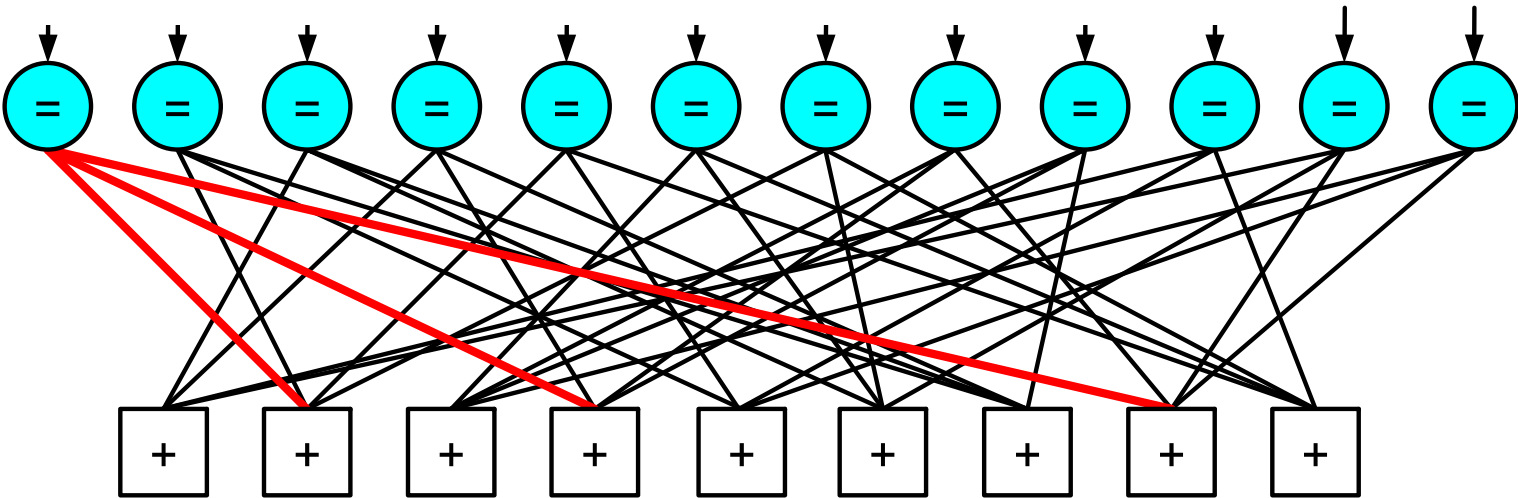
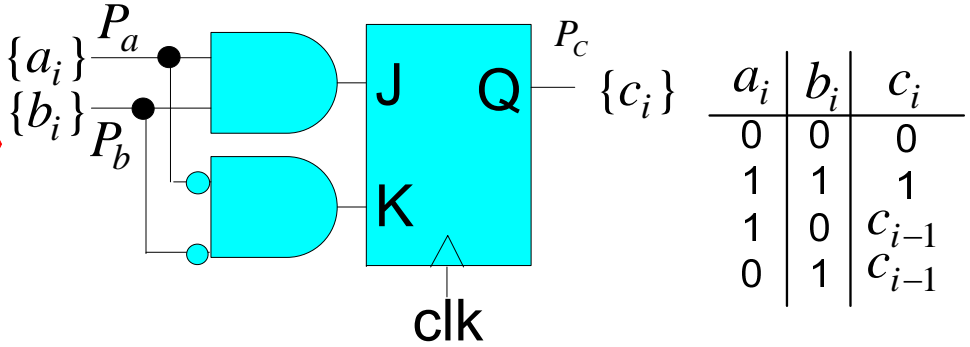
$$P = 0.76 (= 19/25)$$

...01111111100110110111111011...

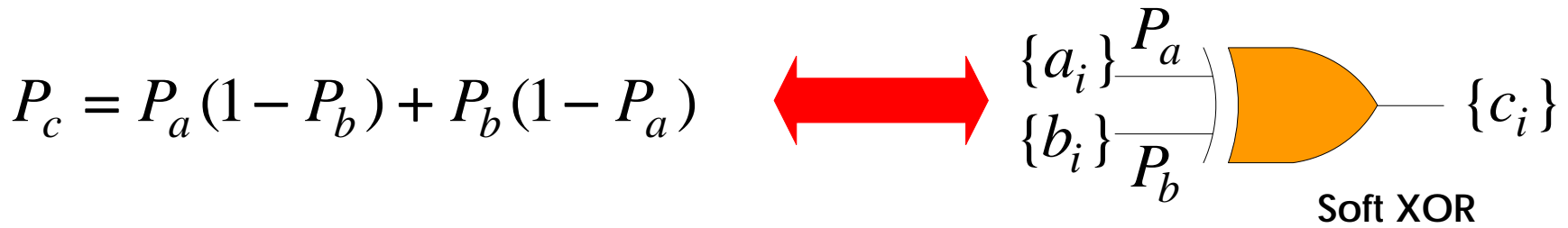
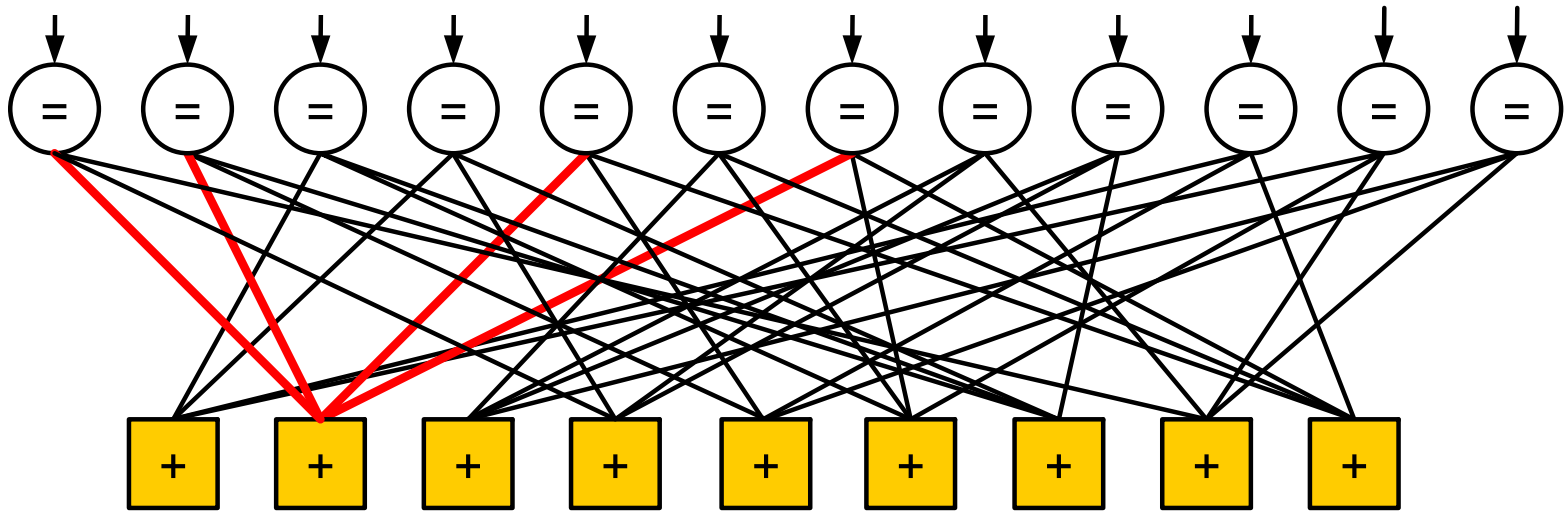
- Encode probabilities as streams of random bits
- Common fallacy: low precision
  - 0.001 (10 bits in fixed-point vs. 1000 bits in stoc)
- Robust applications
  - Care about **flow of changes of statistics** of bits rather than on the precise value in a discrete frame of bits

# Stochastic Variable Node [Gaudet and Rapley, Elec. Letters 2003]

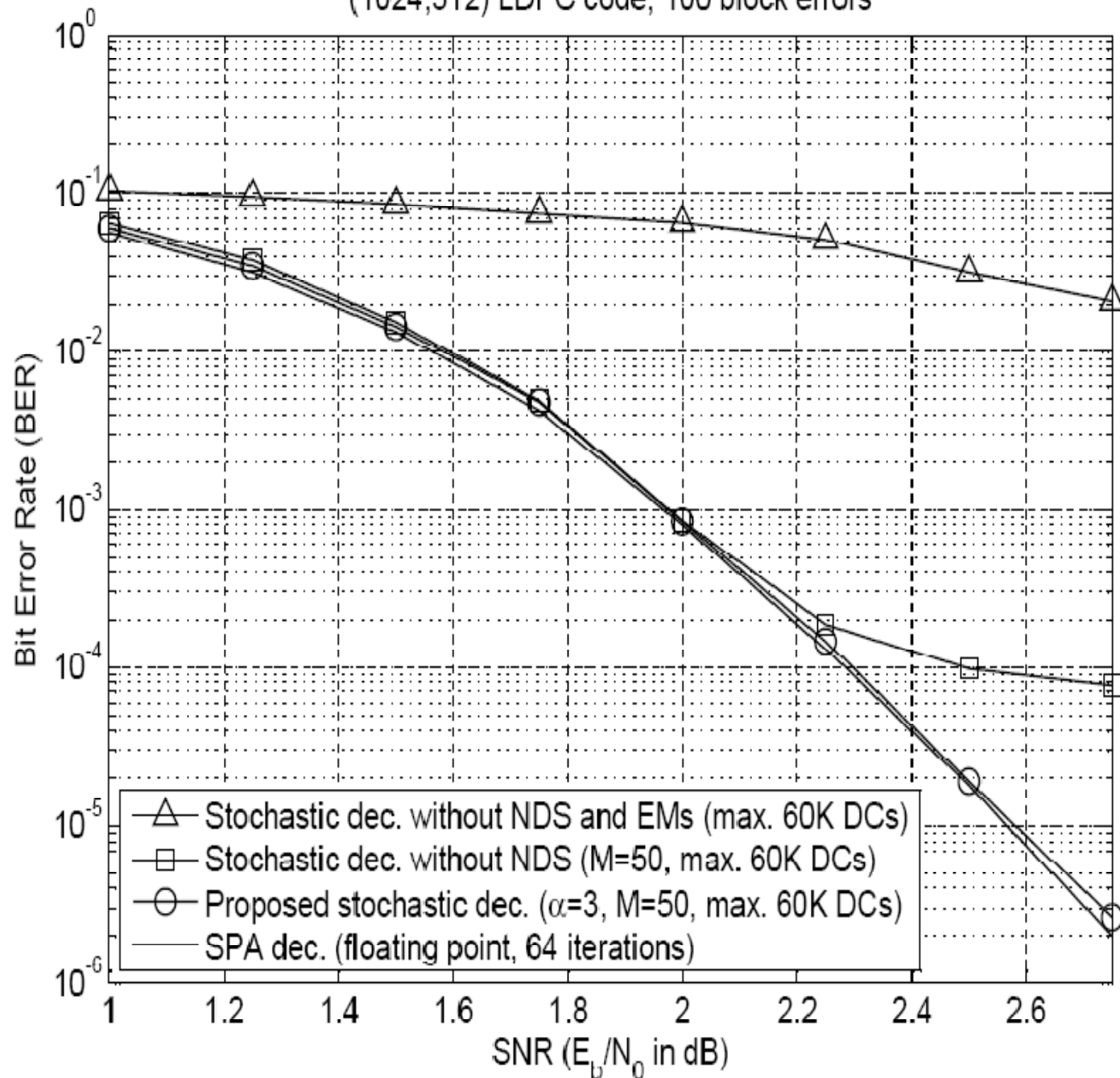
$$P_c = \frac{P_a P_b}{P_a P_b + (1 - P_a)(1 - P_b)}$$



# Stochastic Parity-Check Node [Gaudet and Rapley, Elec. Letters 2003]

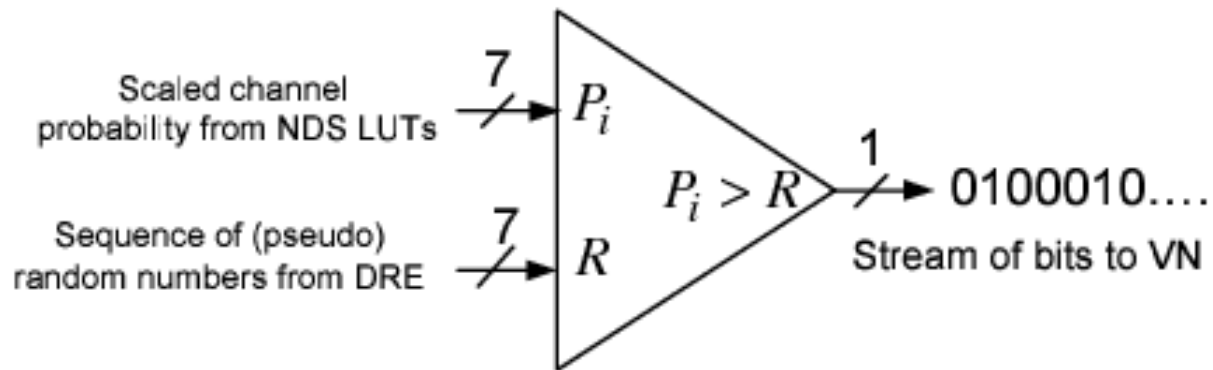


(1024,512) LDPC code, 100 block errors



# *FPGA Implementation*

## *Probability to stochastic conversion*



- *Distributed Randomization Engine provides the random numbers*

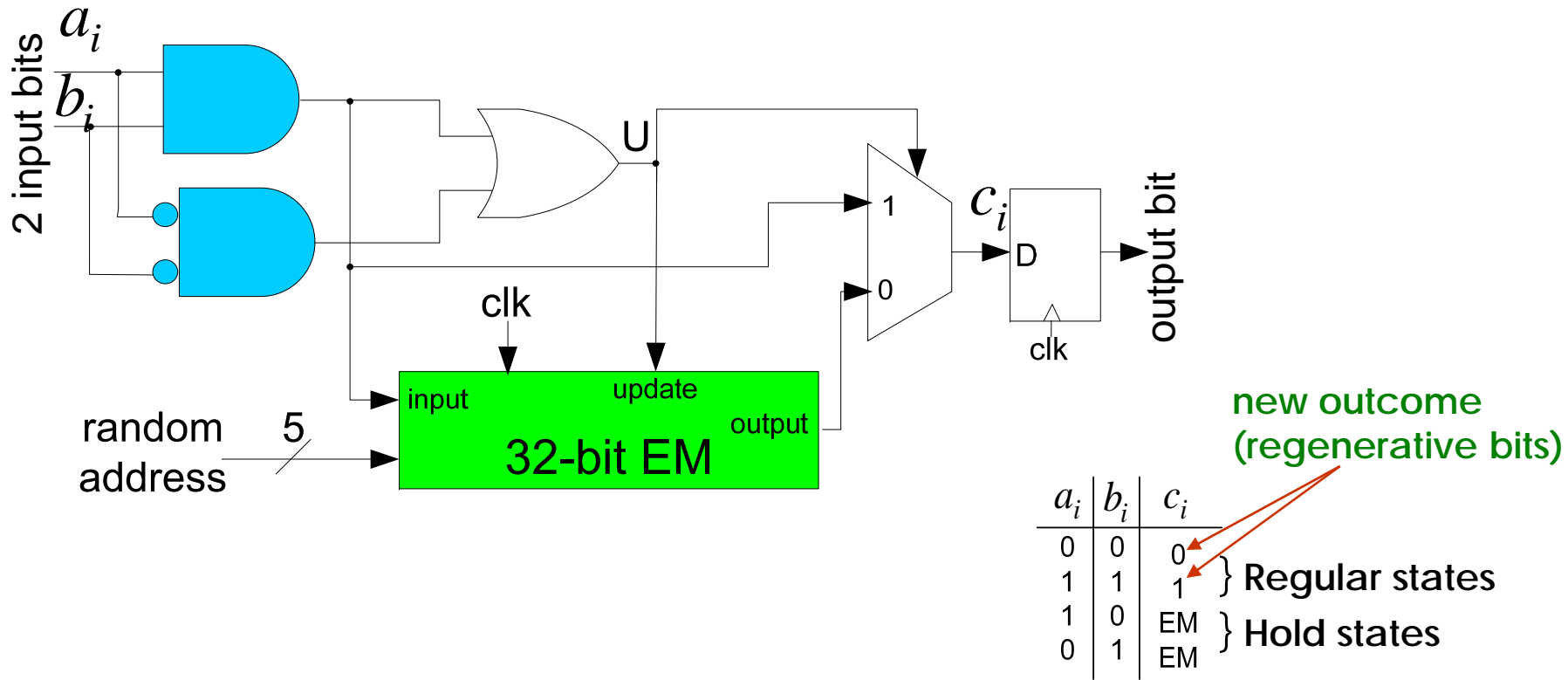
## *Hard-decisions*

- At the end of each cycle the output bit of each equality node is passed to a saturating 6-bit up/down counter:

*counter++*    (if *input=1* & *counter* < *MAX*)

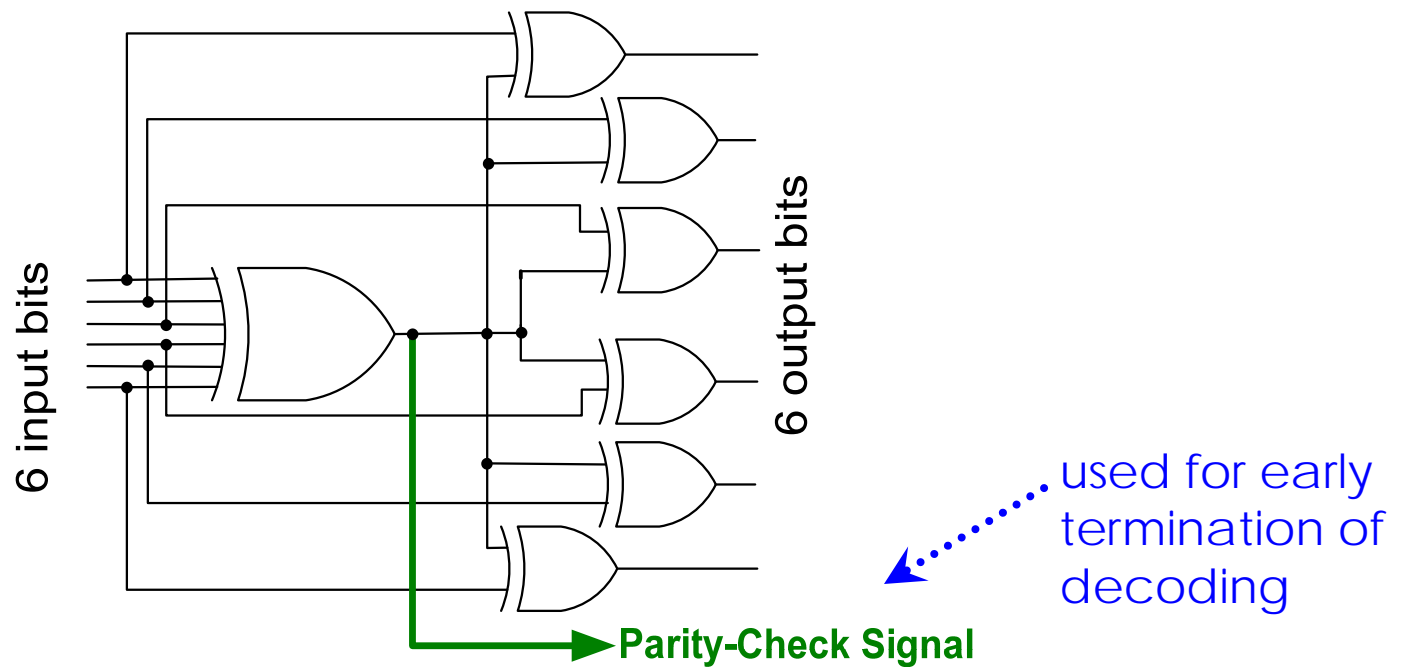
*counter--*    (if *input=0* & *counter* > *MIN*)

# Variable Nodes

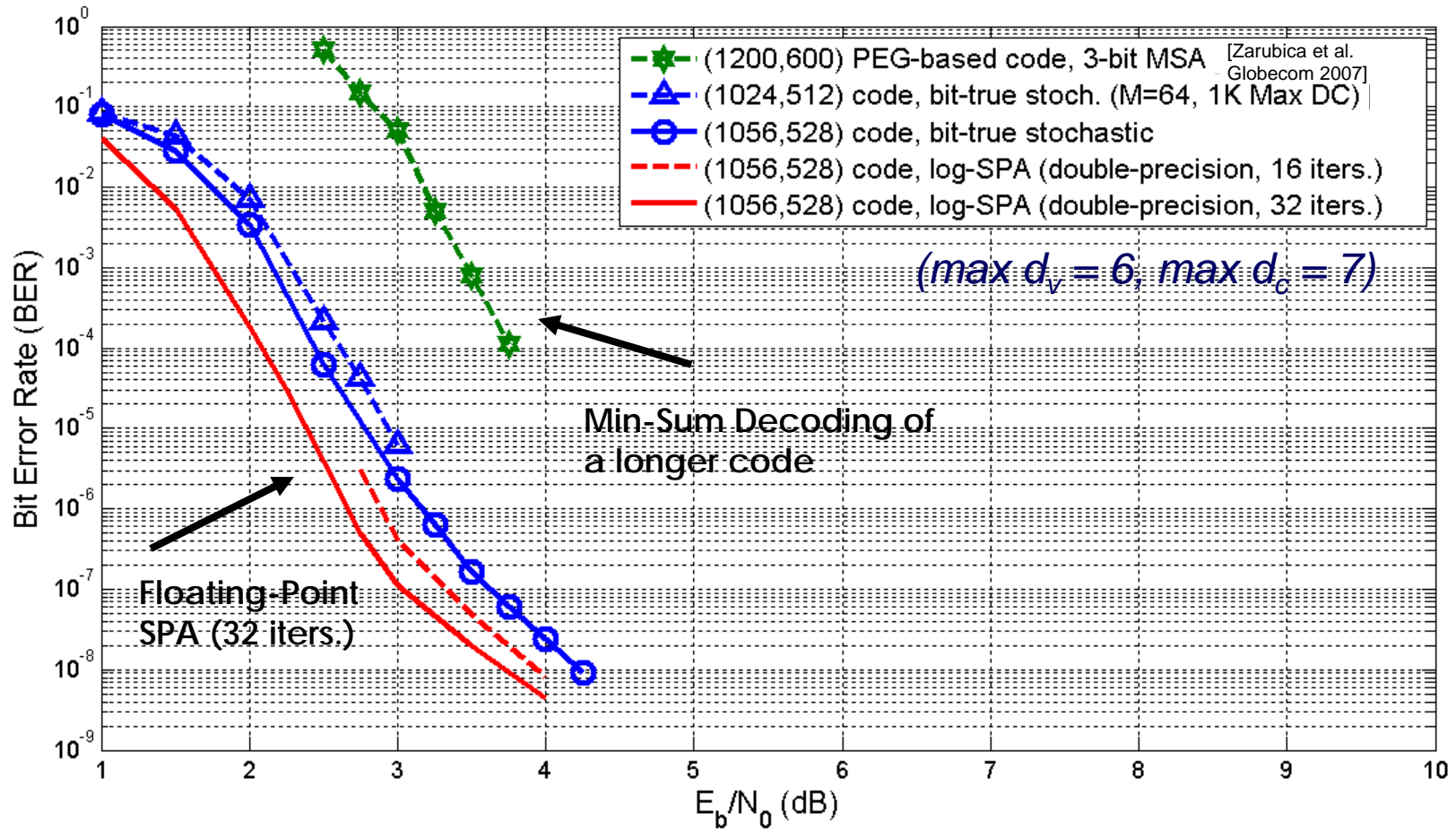


- Significant sharing of random numbers
- Share between comparators / EMs

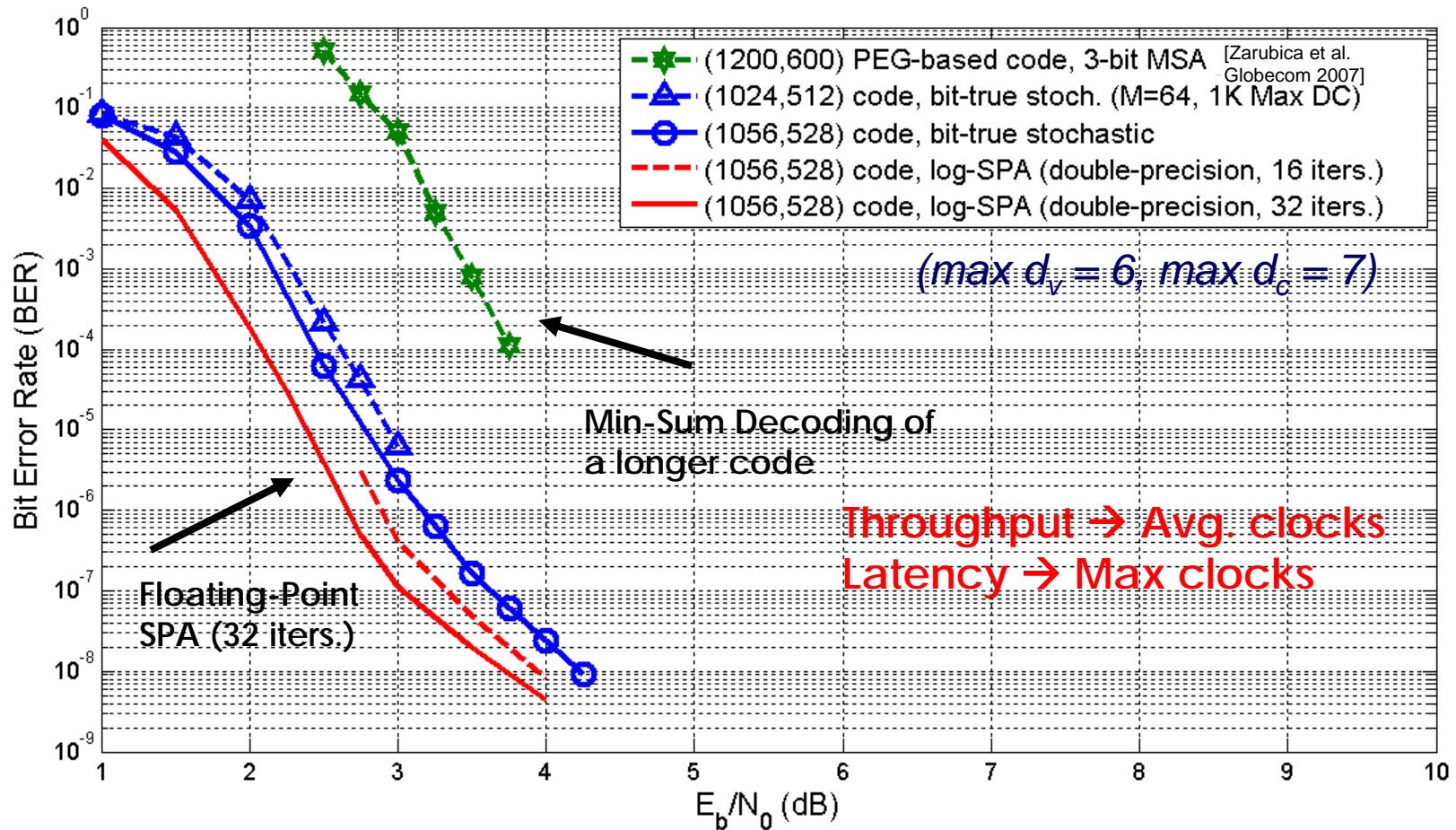
# Parity-Check Nodes



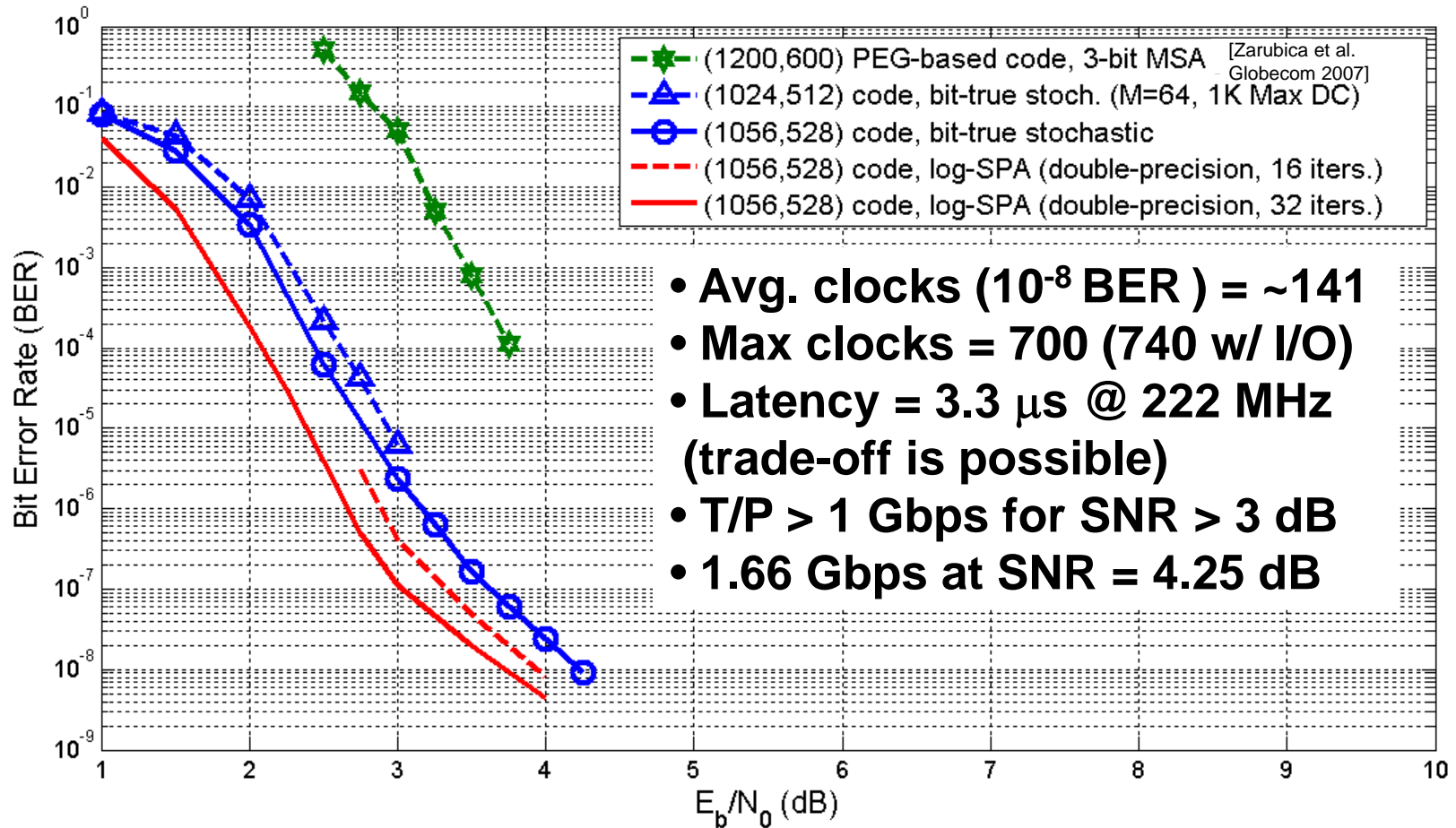
# FPGA Implementation



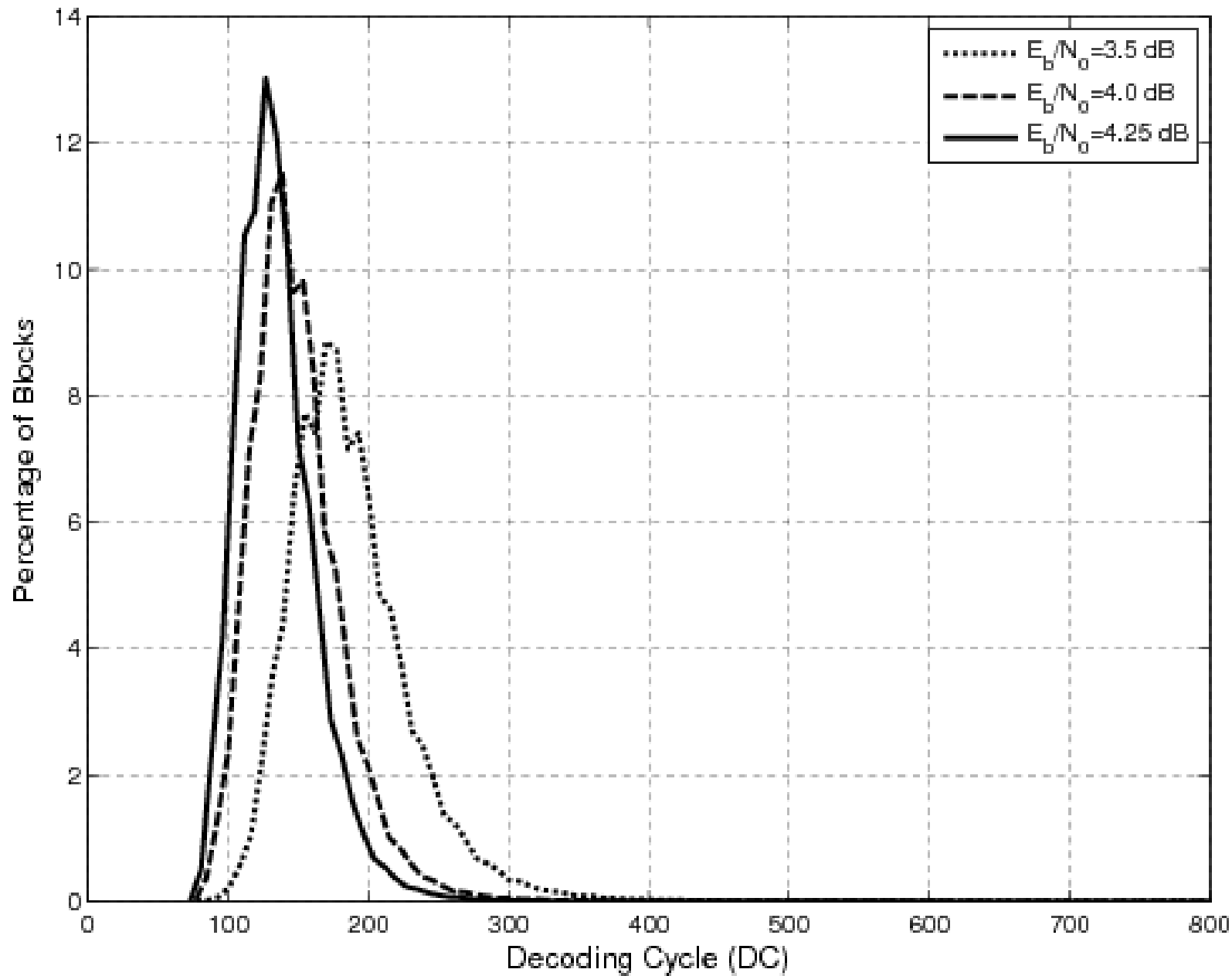
# FPGA Implementation



# FPGA Implementation



(1056,528) WiMAX LDPC code with  $d_v=[2,3,6]$  and  $d_c=[6,7]$

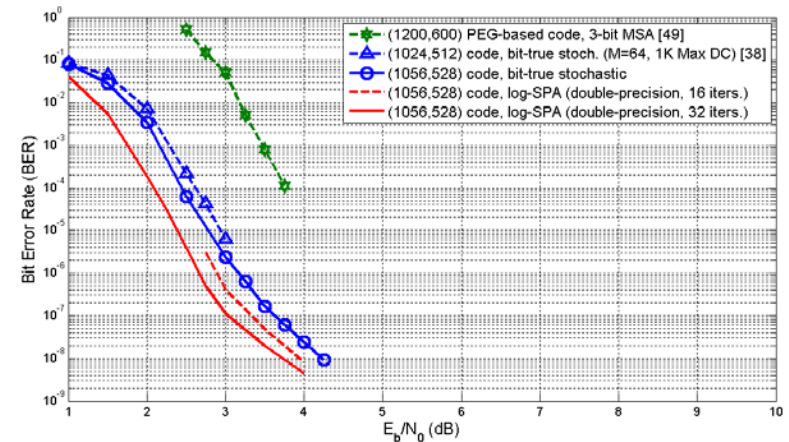


# FPGA Resources

- Xilinx Virtex-4 LX200
- (1056, 528) (max (6,7))-irregular code

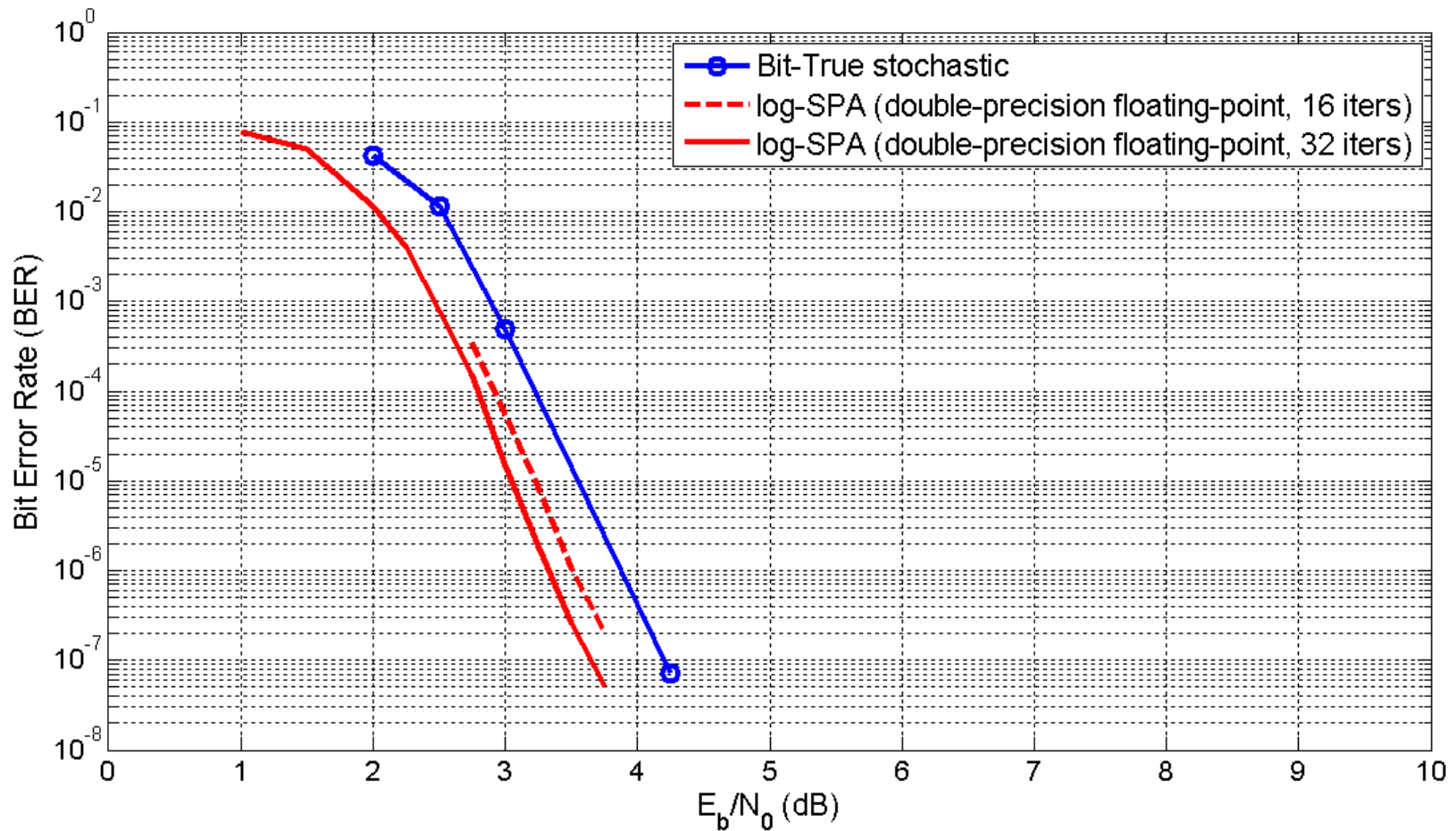
Resources	Occupied	Available	Utilization
Slice LUTs	68163	178176	38%
Slice FFs	44502	178176	24%
IOBs	308	960	32%
Slices	46097	89088	51%

# FPGA Comparison



	Darabiha et al. ISCAS 2006 (bit-serial approx MSA)	Zarubica et al. Globecom 2007 (3-bit MSA)	Sharifi Tehrani et. al. SIPS 2007	Sharifi Tehrani et al. Trans SP, 2008 (sub)
T/P / information bit <b>(Mbps – normalized)</b>	<b>1.83</b>	<b>10</b>	<b>1.38</b>	<b>3.14</b>
Slices / coded bit	<b>69.3</b>	<b>33.8</b>	<b>32.1</b>	<b>43.6</b>

# *(1056, 704) Irregular LDPC*

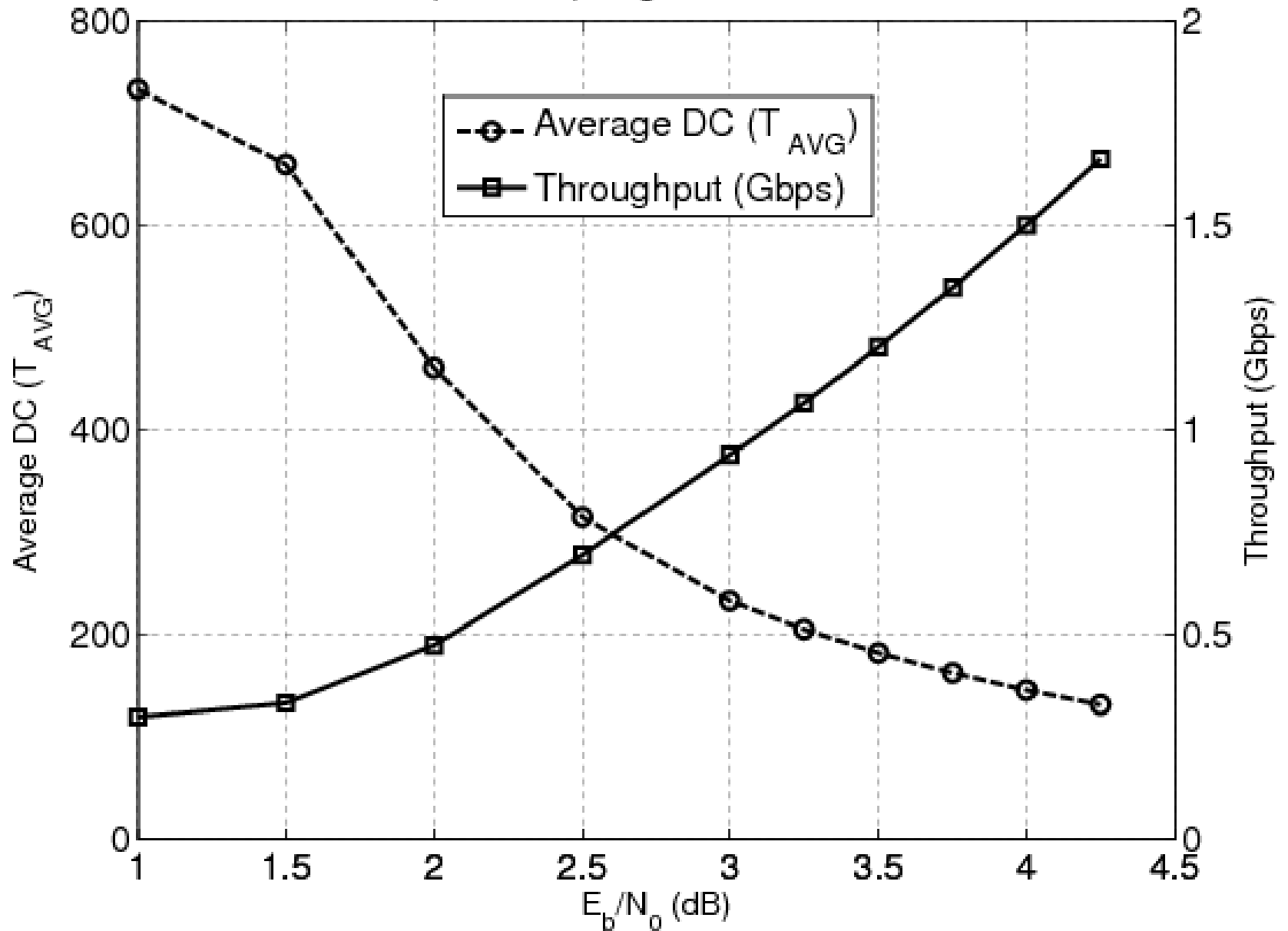


# Conclusions

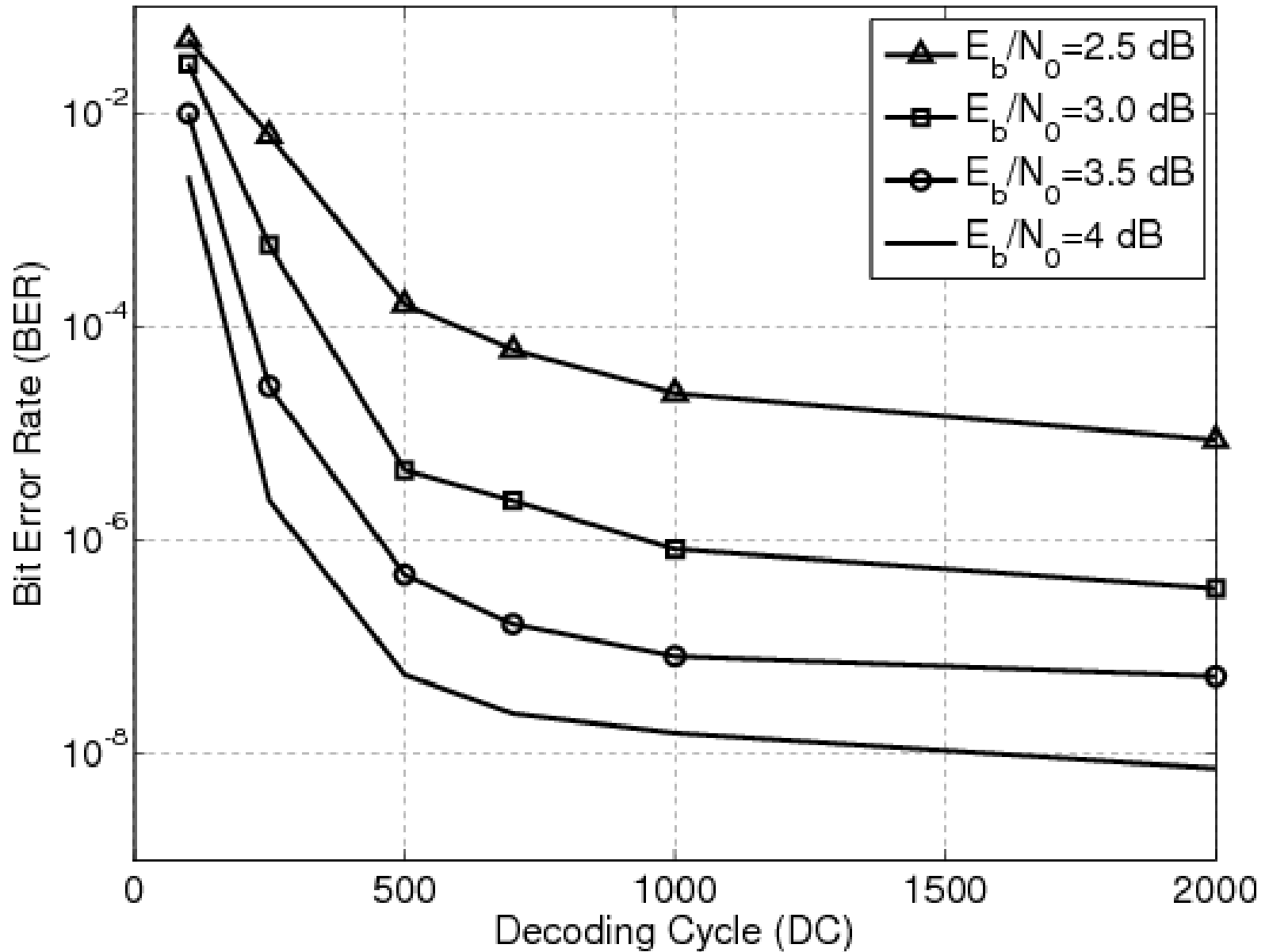
- First irregular fully-parallel LDPC decoder on FPGA
- One of the fastest ( $> 1$  Gbps) and most area-efficient fully-parallel decoders
- Superior error-correcting performance
- Bit-serial interleaver and simple node H/W  
→ efficient ASICs
- Easy, scalable and portable design
- Easy trade-offs
- Potential for very low-power

# *Extra Slides*

(1056,528) irregular LDPC code

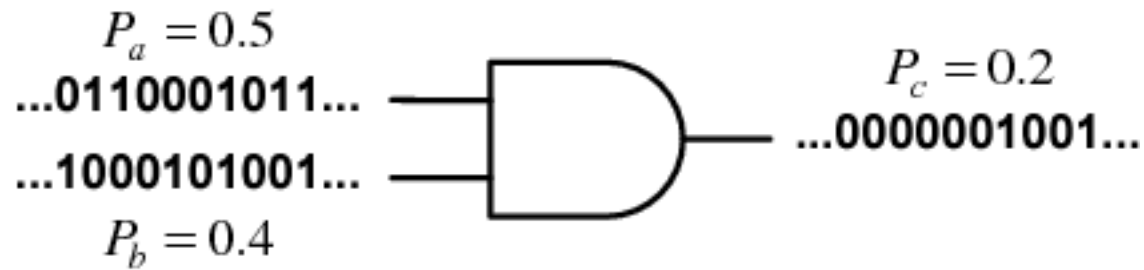


(1056,528) irregular LDPC code

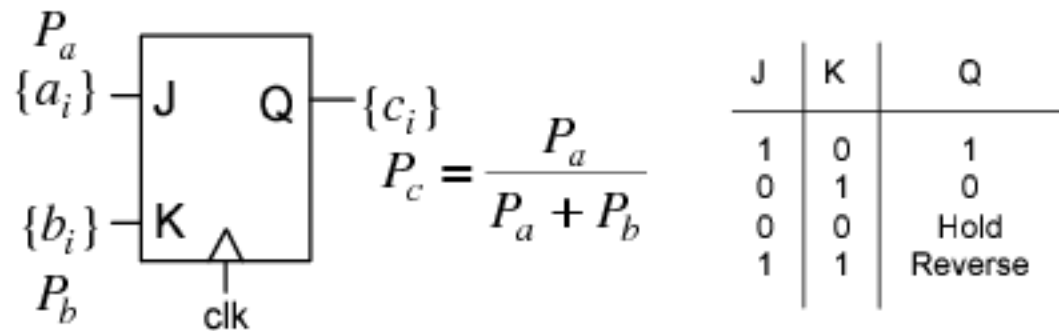


# Comparison

	Fastest non-stochastic FPGA-based decoders		Stochastic decoders	
Code	(480,355)	(1200,600)	(1024,512)	(1056,528)
Code structure	Regular, RS-based	Regular, PEG-based	Regular	Irregular, WiMAX code
max ( $d_v, d_c$ )	(4,15)	(3,6)	(3,6)	(6,7)
Decoding	Bit-serial approx. MSA	3-bit fixed-point MSA	Stochastic	Stochastic
Iterations or DCs	15 iters.	10 iters.	6K and 1K (max DCs)	700 (max DCs)
Input Quantization	3 bits	3 bits	8 bits	6 bits
FPGA device	Stratix EP1S80	Virtex-4 XC4VLX200	Virtex-4 XC4VLX200	Virtex-4 XC4VLX200
Max. Clock	61 MHz	100 MHz	212 MHz	222 MHz
Clocks per iter. or DC	3	1	1	1
Max. latency ( $\mu$ s)	0.73	0.1	28.30 (for 6K max. DCs) 4.71 (for 1K max. DCs)	3.3
T/P per information bit	1.83 Mbps	10 Mbps	1.38 Mbps (at BER $\approx 10^{-6}$ )	3.14 Mbps (at BER $\approx 10^{-8}$ )
4-input LUTs and FFs per coded bit	not reported (worst case: 138.7 LUTs and FFs)	57.5 LUTs and 15.7 FFs	46.0 LUTs and 20.1 FFs	64.5 LUTs and 42.1 FFs
Slices/LEs per coded bit	138.7 LEs ( $\approx 69.3$ slices)	33.8 slices	32.1 slices	43.6 slices
Relative decoding gain (at BER= $10^{-4}$ )	not comparable	-	$\approx 1.1$ dB,	$\approx 1.3$ dB,
Hardware decoding loss (at BER= $10^{-4}$ )	not reported	$\approx 0.25$ dB loss from floating-point MSA (10 iters.)	$\approx 0.2$ dB loss from floating-point SPA (32 iters.)	$\approx 0.4$ dB loss from floating-point SPA (32 iters.)



## multiplication



## division